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Searching 1976-2000...

Results of Search in 1976-2000 db for:

((pipeline AND hypercube) AND header) AND packet): 52 patents.

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PAT. NO. Title

- 1 [6,094,715 SIMD/MIMD processing synchronization](#)
- 2 [6,091,857 System for producing a quantized signal](#)
- 3 [5,966,528 SIMD/MIMD array processor with vector processing](#)
- 4 [5,964,835 Storage access validation to data messages using partial storage address data indexed entries containing permissible address range validation for message source](#)
- 5 [5,963,746 Fully distributed processing memory element](#)
- 6 [5,963,745 APAP I/O programmable router](#)
- 7 [5,914,953 Network message routing using routing table information and supplemental enable information for deadlock prevention](#)
- 8 [5,878,241 Partitioning of processing elements in a SIMD/MIMD array processor](#)
- 9 [5,870,619 Array processor with asynchronous availability of a next SIMD instruction](#)
- 10 [5,867,727 System for judging read out transfer word is correct by comparing flag of transfer word and lower bit portion of read destination selection address](#)
- 11 [5,867,501 Encoding for communicating data and commands](#)
- 12 [5,842,031 Advanced parallel array processor \(APAP\)](#)
- 13 [5,838,894 Logical, fail-functional, dual central processor units formed from three processor units](#)
- 14 [5,832,295 System for detecting the presence or absence of a loss of transfer word by checking reception side judgement bits](#)
- 15 [5,828,894 Array processor having grouping of SIMD pickets](#)
- 16 [5,815,723 Picket autonomy on a SIMD machine](#)
- 17 [5,802,366 Parallel I/O network file server architecture](#)

- 18 5,794,059 N-dimensional modified hypercube
- 19 5,790,776 Apparatus for detecting divergence between a pair of duplexed, synchronized processor elements
- 20 5,765,012 Controller for a SIMD/MIMD array having an instruction sequencer utilizing a canned routine library
- 21 5,765,011 Parallel processing system having a synchronous SIMD processing with processing elements emulating SIMD operation using individual instruction streams
- 22 5,761,523 Parallel processing system having asynchronous SIMD processing and data parallel coding
- 23 5,754,871 Parallel processing system having asynchronous SIMD processing
- 24 5,752,067 Fully scalable parallel processing system having asynchronous SIMD processing
- 25 5,751,955 Method of synchronizing a pair of central processor units for duplex, lock-step operation by copying data into a corresponding locations of another memory
- 26 5,751,932 Fail-fast, fail-functional, fault-tolerant multiprocessor system
- 27 5,734,921 Advanced parallel array processor computer package
- 28 5,721,819 Programmable, distributed network routing
- 29 5,717,944 Autonomous SIMD/MIMD processor memory elements
- 30 5,717,943 Advanced parallel array processor (APAP)
- 31 5,713,037 Slide bus communication functions for SIMD/MIMD array processor
- 32 5,710,935 Advanced parallel array processor (APAP)
- 33 5,708,836 SIMD/MIMD inter-processor communication
- 34 5,689,689 Clock circuits for synchronized processor systems having clock generator circuit with a voltage control oscillator producing a clock signal synchronous with a master clock signal
- 35 5,675,807 Interrupt message delivery identified by storage location of received interrupt data
- 36 5,675,579 Method for verifying responses to messages using a barrier message
- 37 5,625,836 SIMD/MIMD processing memory element (PME)
- 38 5,617,413 Scalable wrap-around shuffle exchange network with deflection routing
- 39 5,611,038 Audio/video transceiver provided with a device for reconfiguration of incompatibly received or transmitted video and audio information
- 40 5,598,408 Scalable processor to processor and processor to I/O interconnection network and method for parallel processing arrays
- 41 5,590,345 Advanced parallel array processor(APAP)
- 42 5,588,152 Advanced parallel processor including advanced support hardware
- 43 5,574,849 Synchronized data transmission between elements of a processing system
- 44 5,524,212 Multiprocessor system with write generate method for updating cache
- 45 5,355,453 Parallel I/O network file server architecture
- 46 5,280,474 Scalable processor to processor and processor-to-I/O interconnection network and method for parallel processing arrays
- 47 5,170,393 Adaptive routing of messages in parallel and distributed processor systems

48 5,163,131 Parallel I/O network file server architecture

49 5,113,523 High performance computer system

50 5,105,424 Inter-computer message routing system with each computer having separate routing automata for each dimension of the network

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